Quality Assurance of Electrostatic Micro-Electro Mechanical Relays: Radiation Hardness

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***Abstract* - As electrostatic Micro-Electro Mechanical relays have the potential to solve power density issues related to current MOSFET technology, it has become ever more important to examine device reliability. Beyond applications on earth, MEM devices could promise to reduce overhead power consumption aboard spacecraft. Thus this paper provides a brief history of radiation hardness in MEM devices. The experimental effects of radiation on device performance are then examined and device degradation is discussed. Finally the efficacy of this technology for industry, in the near future, is gauged.**

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I. INTRODUCTION

Complementary Metal Oxide Semiconductors (CMOS) exist today as the fundamental building block for logic circuits through metal-oxide-semiconductor field-effect transistors (MOSFETs). CMOS technology is widely used in microprocessors, microcontrollers, and static RAM, where millions of MOSFETs are joined to create a chip or chipset. P and N type doping allows CMOS devices to run the logic required by modern processing applications. High voltage differential between a gate and body electrode creates an inversion layer capable of conducting charge between the drain and source electrodes. The voltage required to reach this state, colloquially termed the “on” state, is known as the “threshold” voltage. Low voltage differential, below the threshold voltage, results in low conductivity and a state known as the “off” state. These states underpin the binary logic used as the fundamental building blocks of nearly all microprocessors. As such, CMOS devices and technology are the limiting factor in any discussion of modern technological efficiency.

The predominant challenge facing current cmos technology revolves around fundamental lower limits of energy usage. Considering the expansive amount of these devices employed today, even marginal energy consumption levels per device result in extreme global

demands. The predominant method to reduce dynamic energy consumption involves a decrease in supply voltage but doing so results in increased circuit delay. In order to avoid this outcome, threshold voltage must be decreased in conjunction with supply voltage. However, a decrease in threshold voltage results in increased off-state leakage current (known as sub-threshold leakage) and thereby an increase in static energy consumption. Minimization of total energy must require a balance of dynamic and static energy which creates a fundamental lower limit on the energy efficiency of CMOS devices.

These fundamental lower limits on device performance can be further scaled in devices with low performance demands or high levels of parallelism[1]. In these applications performance (measured by supply voltage over current) can be more rigorously scaled due to the single importance of a minimum supply voltage as opposed to overall high end performance. However in critical applications these methods are not an option and thus power density remains problematic. In short, current CMOS technology cannot hope to sustain the exponential increase in high-end consumer electronics because of the off-state leakage current associated with these devices. In this context nanoscale relays present themselves as an attractive alternative for alleviating CMOS power consumption limitations.

Nanoscale relays are beneficial from a static energy consumption standpoint due to their lack of an off-state leakage current. The fabricated device contains an air gap between source and drain which can only be actuated by a drive voltage between the body and gate. In the off state no path exists for current to flow and thus there is no leakage associated with nanoscale relays. The geometry of the devices would require ionization of the air gap in order for current flow, an outcome which is highly hindered at low voltages. This reality allows aggressive scaling of the source voltage as well as the threshold voltage due to the lack of increase in static energy consumption. In nanorelays source voltage can theoretically be scaled solely as a function of required device performance and functionality.

As described by Spencer et. Al., from a performance standpoint, two major problems surround current relay technology. First, relays exhibit large switching delays, on the order of nanoseconds, several orders of magnitude larger than those of CMOS devices which switch on the order of picoseconds. Specifically, relays in the 90 nm technology range are likely to have delays nearing 10 nanoseconds while current transistor technology exhibits delays in the range of 100 picoseconds. Redesigning circuit topology for nanorelays would alleviate this problem by forcing all mechanical movement to happen simultaneously. Although this would increase electrical delay at the

device level, at the circuit level it would theoretically promote efficiency on a level comparable to that of current CMOS technology.

Secondarily, for relay technologies to replace those of CMOS, increased device reliability is required. Devices must be capable of functioning in the range of 10^{14} on/off cycles before failure in order to achieve the longevity associated with CMOS devices[1]. This standard is many orders of magnitude greater than that displayed in the most durable micro-electrical mechanical relays to date. However recent reliability testing has achieved upwards of 60 billion cycles before failure[1]. Improved research and scaling in this area suggests such concerns will likely be alleviated in coming years[1].

Scaling of energy-delay characteristics for MEM relays appears extremely promising. Recent modeling indicates that relay technology offers greater than an order of magnitude reduction in energy per operation compared to current CMOS technology[1]. Comparisons of 32-bit adders built from CMOS and MEM relays exhibit the expected mechanical delay as well as greater area needs for MEM devices. However energy-delay characteristics over a wide range of frequencies appear nearly an order of magnitude better for the MEM relays. This further validates the feasibility of MEM relays as an energy efficient alternative to CMOS technology in integrated circuits. Additional

scaling to the nano-level can likely improve other performance concerns of this technology[2]. Increased parallelism in circuit level design for MEM devices is thought to be capable of dramatically alleviating energy concerns.

Device Structure

Fig. 1 shows a diagram of the MEM relay used in this work. The six-terminal device consists of a poly-SiGe gate suspended by four spring-like flexures. Below the gate two pairs of drain and source electrodes protrude upward, between which a tungsten body electrode is positioned. Two channels on the bottom of the gate, composed of tungsten attached to an insulating oxide layer, span the gap between each source and drain electrode. Two dimples on the bottom of each channel define where contact is made on the source and drain. A thin titanium oxide (TiO_2) layer coats the device to protect against formation of tungsten oxides. An aluminum oxide dielectric layer is positioned directly under the gate on each device with an approximate thickness of 50nm.

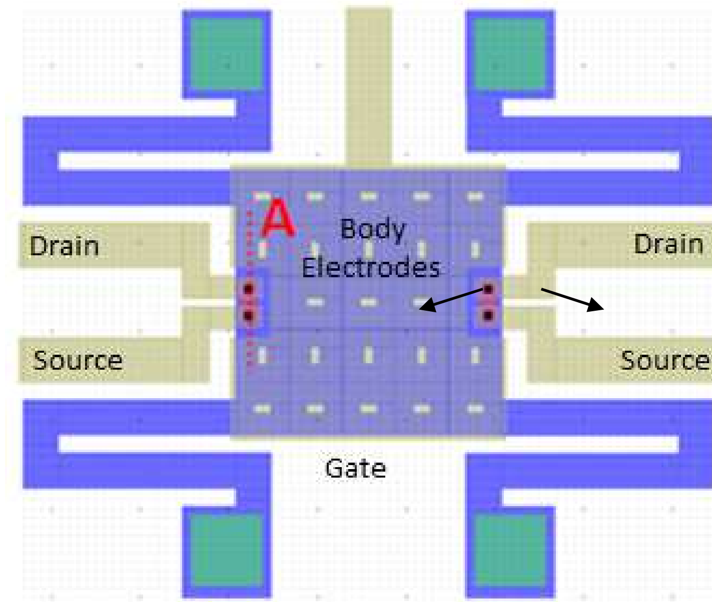

Fig.1A Schematic View – Depicts the aerial layout of the 6T devices. The pink sections designate the interchangeable source and drain electrodes. Cross section A is drawn in for reference.

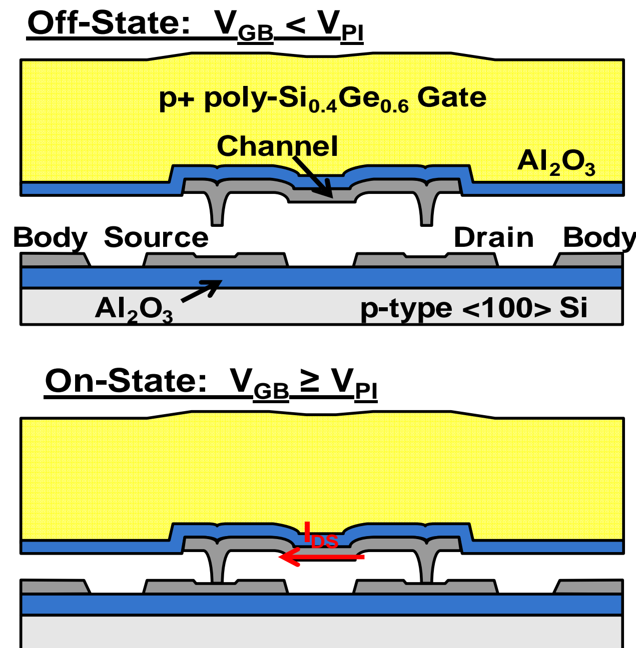

Fig.1 6T Relay Physical Structure – Depicts the cross section A difference between the off-state and on-state of a MEM relay. The on-state demonstrates contact made between the source and drain electrodes through the channel[1].

Basic operation of the MEM relay depends on applied voltage. A sufficient voltage applied between the gate and body creates an electrostatic force which may overcome the spring effect of the flexures. This process effectively displaces the gate vertically, bringing each channel in contact with a drain and source. The device is defined as being 'on' when this current path exists between each source and drain. Ideally the effect of both channels fixed to a single gate is the simultaneous activation of both sides when the gate is displaced sufficiently. To boost structural integrity and to prevent collapse of the device the dimples in the channel prevent additional gate motion once

contact is made with the drain and source. Sufficient reduction of the gate to body voltage differential results in the spring force surmounting the electrostatic force. This returns the device to its off-state position and subsequently drops leakage current to immeasurable levels. The basic functions of this device can accurately be described with a classical electro-mechanical model[1].

As noted by Spencer et al., a non-linear second-order differential equation can be used for the purpose of modeling the movement of the gate under applied electrostatic force. A spring-mass-damper system considers the mass and flexures as controls for the variable resistances between channel, drain, and source:

$$m\ddot{x} = F_{elec}(x) - b\dot{x} - kx$$

Equation 1

where b is the damping coefficient, x is the displacement of the gate, k is the spring constant of the flexures and $F_{elec}(x)$ is the electrostatic force applied between the gate and body. By neglecting all other fields the electrostatic force can be simplified to only the force between the gate and body

$$F_{elec}(x) = \frac{\varepsilon_O A_{OV} {V^2}_{gb}}{2(g_O - x)^2}$$

Equation 2

where $\varepsilon_0$is the permittivity of free space, A_{OV} is the area of the overlap between the body and gate electrodes, g_0 is the gap between the electrodes absent electrostatic force, and $V_{gb}$is the applied voltage. During the actuation of the device the spring force will vary linearly with the displacement of the gate. The electrostatic force is inversely quadratic to the same displacement and therefore results in a critical displacement being reached. At this point the device enters into a range where the difference in forces causes the device to spontaneously snap shut, and activate.

The gap at which the spring and electrical forces are equal is known to be one third of the overall gap distance. Pull-in voltage (V_{pi}) can therefore be calculated[1]:

$$V_{pi} = \sqrt{\frac{8}{27} * \frac{k{g^3}_0}{\varepsilon_0 A_{OV}}}$$

Equation 3

As expected, a larger gate to body voltage differential results in larger electrostatic force, greater acceleration, and a shorter mechanical delay. Additional scaling of the device drives the down necessary V_{pi} through a decrease in the spring force constant k.

Model concerns due to environmental factors are largely misplaced. The extremely low mass of the MEM devices dictates a low moment of

inertia. This reality makes it nearly impossible to actuate the device via external vibration and acceleration. For instance, the devices measured in this work would take upwards of 20,000 g in order to actuate externally through counteraction of the spring force. Additional scaling promises increased immunity to these factors. Likewise thermal energy presents minimal risk to MEM relays. The structures are confined to a single degree of vertical freedom or $\frac{k_B T}{2}$ joules of thermal energy. Considering the $\frac{kx^2}{2}$ joules of stored spring potential energy, thermal energy displacement can be shown to amount to roughly 8pm or 0.005% of the actuation gap. Thus both external acceleration and thermal energy present negligible variance in pull-in voltage. This allows for accurate measurement and comparisons of V_{pi} between devices[2]. Likewise, device degradation testing is made possible via consistent V_{pi} functionality.

Of the areas where MEM devices might be of the most practical use, space exploration appears at the forefront of consideration. Space flight has historically become ever more ambitious in both its reach and duration. This scaling of orbital technology has been enabled by low power consumption devices through a parallel scaling of CMOS technology. Unfortunately current CMOS transistor technology has fundamental lower limits which cannot be further alleviated through

optimization techniques. This reality is a direct product of the sub-threshold leakage inherent in CMOS devices. In recent years sub-threshold voltage of CMOS devices has been optimized to balance leakage energy and dynamic energy; additional reductions in the sub-threshold voltage therefore have the unfavorable effect of increasing overall power consumption.

To circumvent these problems micro-electro-mechanical (MEM) relays are being increasingly examined as a viable replacement for space technology. The immeasurably low leakage currents offered by these devices promise potential scalability beyond the lower limits of CMOS transistors. Recent examples of energy-delay characteristics in which MEM relays were found more efficient than their CMOS counterparts have further served to validate these devices' potential in industry[1]. However, in energy-critical applications such as space exploration many questions of reliability remain untested. Paramount to device viability in space is the question of radiation hardness. The spaceflight environment results in a higher level of radiation than that experienced on earth. Although this rate is not constant, often varying six orders of magnitude, devices must be required to withstand substantial irradiation over time.

To date few radiation tests have been performed on MEM devices. Of the experiments that have been conducted the majority pertain to optical mirrors, accelerometers and electrostatic pistons. Studies on these devices from Sandia National Lab report fidelity up to 10 MRads but are not focused on such cantilever designs as used in MEM relays. Moreover tested devices often did not contain dielectric layers and were often activated via thermal or piezo-electric means, making them substantially different from MEM relays. This leaves a particular literature gap in the area of electrostatic relays exposed to the effects of radiation and thereby increases the difficulty of predicting outcomes of such an experiment.

Fortunately, electrostatically actuated pistons and RF switches share fundamental workings with MEM relays. Both are electrostatically activated as opposed to thermally or piezo-electrically activated. MEM pistons and switches additionally contain dielectric layers, which are an important consideration when undergoing irradiation. Finally, MEM pistons and switches can be scaled to levels comparable to that of the MEM relays considered in this work. Thus current literature on the subject can be used to extrapolate the effects of radiation on the MEM relay devices. Likewise current literary solutions may be used to guide future MEM relay developement.

Most research to date suggests that radiation exposure promotes various effects in the electronic properties of MEM devices. Shea[2] thoroughly examines the physical effects of radiation on electrostatic MEM devices. Silicon as a structural material is thought to be radiation hard which suggests most MEM devices will be by default. Despite measuring variations in pull-in voltage among devices, findings conclude that the Young's Modulus for electrostatic MEM remains unchanged after high-end irradiation. This suggests that the damage to MEM devices is not caused by *"bulk damage"* or physical defects. Instead the electronic structure of MEM devices is most likely responsible for device failure. Key considerations include the proximity of dielectric layers to mechanical parts as well as the level of shielding involved.

Caffey[3] suggests that electronic disruption from radiation is due instead to electron-hole pair creation. Hole-pairs are easily created and trapped, in dielectric layers, by relatively minor amounts of radiation. The net effect of electron hole-pairs being trapped in this way is an electric field emanating from the, now positively charged, dielectric layer. This field creates a semi-permanent electrostatic force on the mechanical workings on the device. Such a force has the potential to alter electronic properties in MEM devices; in the case of the electrostatic pistons this effect results in an increased voltage

necessary for pull in. However, McClure[4] finds that alternative geometries, wherein the dielectric layer was not as proximal to moving parts, severely mitigated this effect. RF switches showed little change in operation for doses up to 150 kRad for one design but for a separate design device performance started to degrade around 10 kRad[5]. The more proximal layer in the latter device allowed charge build-up to more easily affect mechanical parts. These findings suggest that dielectric layer proximity to mechanical devices is the primary concern for radiation testing.

A substantial charge build-up in a dielectric layer has the potential to severely increase device V_{pi} and thereby decrease energy efficiency. The pull-in voltage is that necessary to overcome the spring force (kx) through generation of a counteracting electrostatic force. A dielectric layer will polarize throughout this process but will generally have little effect on the mechanical functions of the pull in. Charge accumulation suggests that the surface of the dielectric layer becomes positively charged as holes are trapped against the silicon-air interface. This can have one of two effects on the mechanical motion of the device. If the body-gate voltage differential is such that the body is relatively positively charged then the device runs a substantial risk of spontaneous pull in. Conversely, as per the devices used in this paper, if the body has a relative negative charge the charge

accumulation tends to resist the pull in voltage. The consequence becomes a much higher V_{pi} required for activation which limits energy efficiency.

Methods to mitigate the effects of charge accumulation are well known but have yet to be adapted to MEM relays. In spacecraft, a high level of shielding is often conferred by the physical encapsulation of the vehicle in question. This grants most electronic devices on board a preliminary line of defense against radiation. Alpha and beta radiation have little capability of passing through the hull of a spacecraft, leaving only the low ionizing potential of gamma particles. As suggested above the physical location of the dielectric layer additionally plays a role in device degradation. Device design focused on less proximal dielectric layers can severely mitigate the performance degradation even at high dosage[3]. Additional preventative methods such as charge dissipation layers and geometric reorientation are known but exist outside of the scope of this paper.

Additional mitigation occurs through natural charge dissipation via a process known as annealing. The ionization process through which electron hole-pair accumulation occurs is known to be reversible as a function of time. Excess electrons will randomly encounter holes and the electron hole pair will annihilate itself. This process reduces the

charge held in the dielectric layer and over time is thought to return MEM devices to pre-irradiation levels. Thus sufficiently low ionization can be mitigated and reversed, within hours, through the annealing process. Although preventative measures exist as a major focus of radiation hardness, remedial measures are also a noteworthy factor.

For the purposes of this paper three different MEM relays were used. These devices were all six-terminal devices consisting of one gate, one body, two drain, and two source electrodes. They varied only in regard to their physical dimensions which consisted of gate area and flexure size. The devices were termed "series A", "series B" and "series C" in order of decreasing area. The A series had gate area of 30nm x 30 nm, the B series a gate area of 22nm x 22nm and the C series a gate area of 15nm x 15nm. Four devices per series per chip were tested in order to obtain accurate mean data. Each device was analyzed in triplicate before and after irradiation by an alpha particle source. Devices were primarily tested for V_{pi} degradation as function of irradiation; though annealing time was also examined.

Section II highlights the experimental method, especially detailing the radiation levels used and modeling attempts. Results are included in Section III with a focus on pull-in voltage vs. radiation and pull-in

voltage vs. time after radiation. Finally section IV concludes with analysis on the viability of MEM relays for space in the near future.

II. EXPERIMENTAL METHOD

To test for radiation hardness, pull-in voltage degradation was examined over time after initial radiation doses. Thirty-six irradiated devices and twelve control devices were tested periodically after initial radiation and classified. The three separate doses were used respectively on three separate chips which had identical series A, series B, and series C devices. The final chip also contained identical series A, series B, and series C devices but did not undergo any form of radiation treatment. Testing times were 6, 30, 54, 102, and 174 hours after irradiation. Each device was tested in triplicate before radiation and then in triplicate at each subsequent time interval after irradiation.

Alpha particles were chosen because of their low harm potential to humans. Although they cannot pass easily through multiple epidermal layers they were thought to be capable of penetrating the multiple micrometer encasing used for the MEM relays. In addition, the high ionizing potential of alpha particles suggests that very few particles would need to penetrate the incasing in order to see large electron hole-pair generation. Although alpha particles would not be capable of penetrating space shuttles they carry a high ionization potential. The gamma radiation capable of penetrating the hull has much lower

ionization capabilities by comparison. Considering the high-magnitude orders of alpha radiation, devices would likely be capable of existing in space should they withstand this treatment.

The amount of charge trapped due to radiation can be theoretically determined if both the material and dose are known. The electron-hole density per rad(Al_2O_3) can be defined as:

$$\frac{Pair\ Density}{Rad(Al_2O_3)} = \frac{100\,\frac{ergs}{Grad}\,\rho}{\left(10^7\,\frac{ergs}{J}\right)\left(1.6\ x\ 10^{-19}\,\frac{J}{eV}\right)E_p}$$

Equation 4

where ρ is the density of the aluminum oxide layer in grams per cubic centimeter and E_p is the pair generation energy for Al_2O_3 in electron volts[4]. Considering a density of $3.69\ \frac{g}{cm^3}$ and a pair generation energy of $9.4\ eV$, the pair density per rad(Al_2O_3) is approximately

$$\frac{Pair\ Density}{Rad(Al_2O_3)} = 24.5\ x\ 10^{12}\ \frac{pair}{cm^3 * rad(Al_2O_3)}$$

Equation 5

considering an equivalence of $1.602\ x\ 10^{-19}\ \frac{Coulomb}{Hole}$ the stored charge is equal to

$$= \ 3.925\ x\ 10^{-6}\ \frac{Coulombs}{cm^3 * rad(Al_2O_3)}$$

Equation 6

Replicas of each type of device were tested under three distinct alpha particle doses: $1\ x\ 10^{13}\ \frac{ions}{cm^2}$, $3\ x\ 10^{14}\frac{ions}{cm^2}$, and $1\ x\ 10^{15}\ \frac{ions}{cm^2}$. An additional set of devices was reserved as a no-dose control. Converting the ion flux passing through each device into rads and employing the stored charge formula produces a radiation model for MEM devices. Dosage is shown in figure 2.

	Dose A	Dose B	Dose C
Total Ion Flux	$1\ x\ 10^{13}\ \frac{ions}{cm^2}$	$3\ x\ 10^{14}\ \frac{ions}{cm^2}$	$1\ x\ 10^{15}\ \frac{ions}{cm^2}$
Total Rads	$7.4\ x\ 10^{8}\ \frac{rads}{cm^2}$	$2.2\ x\ 10^{10}\ \frac{rads}{cm^2}$	$7.4\ x\ 10^{10}\ \frac{rads}{cm^2}$

Fig.2 – Radiation Doses – Doses used on each device are depicted as well as their equivalent Rad values.

III. RESULTS

Non-irradiated control devices were tested before and after radiation in order to calculate error. However, these devices exhibited unexpected, yet consistent, variations in pull-in voltage (V_{pi}) from one test to the next. The A series devices, for instance, exhibited a uniform 1.5V increase in Vpi from pre-irradiation testing to six hours post irradiation testing. B devices show very little variation over the same period while C devices increased uniformly by 0.5V.

Additional tests on separate experimental control devices over separate time intervals resulted in similar findings. These results indicate additional electrical phenomena occurring apart from radiation. However, this allowed for the control groups to be used as a baseline against the irradiated samples. All data points were sanitized by subtracting the percent change in the control groups from the variation in the test groups.

Low Dose devices ($1\ x\ 10^{13}\ \frac{ions}{cm^2}$) exhibited the least amount of cohesion after being sanitized. Low Dose type B and C devices both showed a 10% V_{pi} increase peak approximately thirty hours post radiation, yet both dramatically decreased thereafter. Low dose type A devices demonstrated an opposite trend and decreased their requisite V_{pi} by nearly 10% after thirty hours. Considering that physical dimensions

are the only differences between these devices, the variation is attributed to natural non-radiation phenomena. It is possible that the charge build-up in Dose 1 devices was heavily shielded by the gate leading to only non-radioactive phenomena taking place. Unfortunately seemingly random 500mV swings in V_{pi} for Dose 1 devices made it impossible to detect any minor variations that occurred.

Dose 2 devices demonstrated a more expected trend. All three devices displayed an initial spike in voltage as measured six hours post-radiation (figure 3a). Both the B and C devices proceeded to anneal after the six hour peak, leading back towards post irradiation V_{pi} levels. Type A devices had a V_{pi} peak after thirty hours which decreased at each subsequent measurement.

Dose 3 devices exhibited the most significant trend. All three types of devices experienced an initial increase in V_{pi} as measured six hours post radiation. Each device then demonstrated a decrease in V_{pi} during each subsequent measurement (figure 3b).

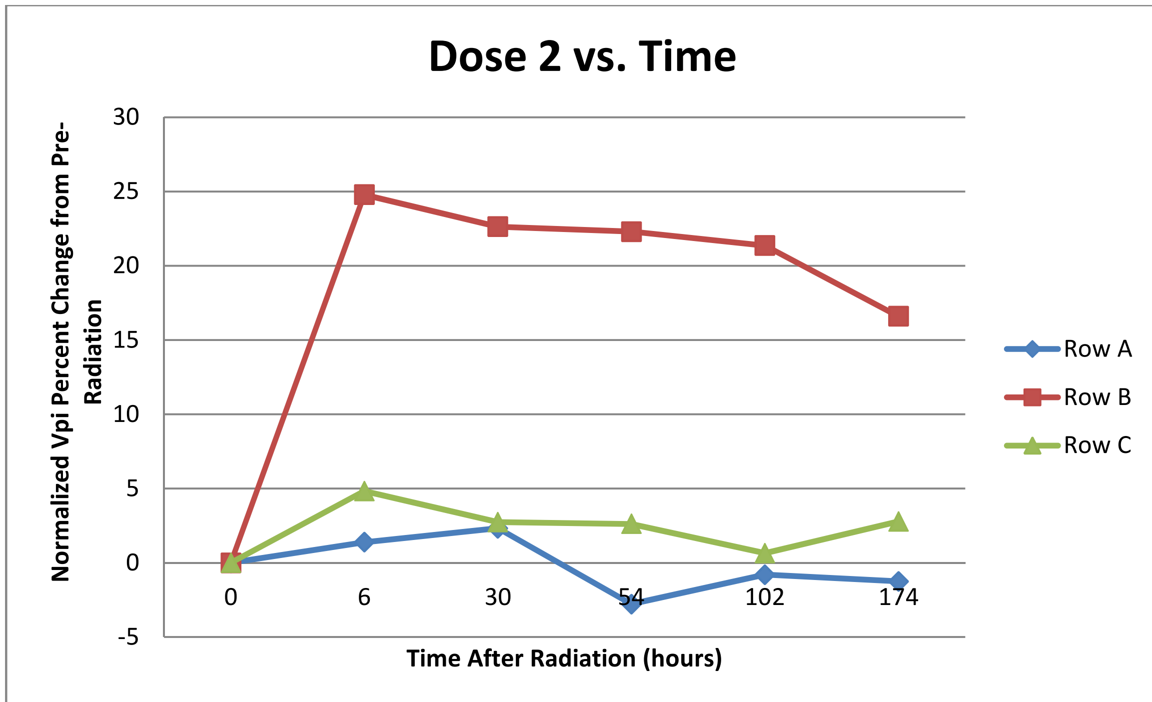

Fig.3a Dose 2 Radiation – Dose 2 devices showed a much greater trend than the original dose.

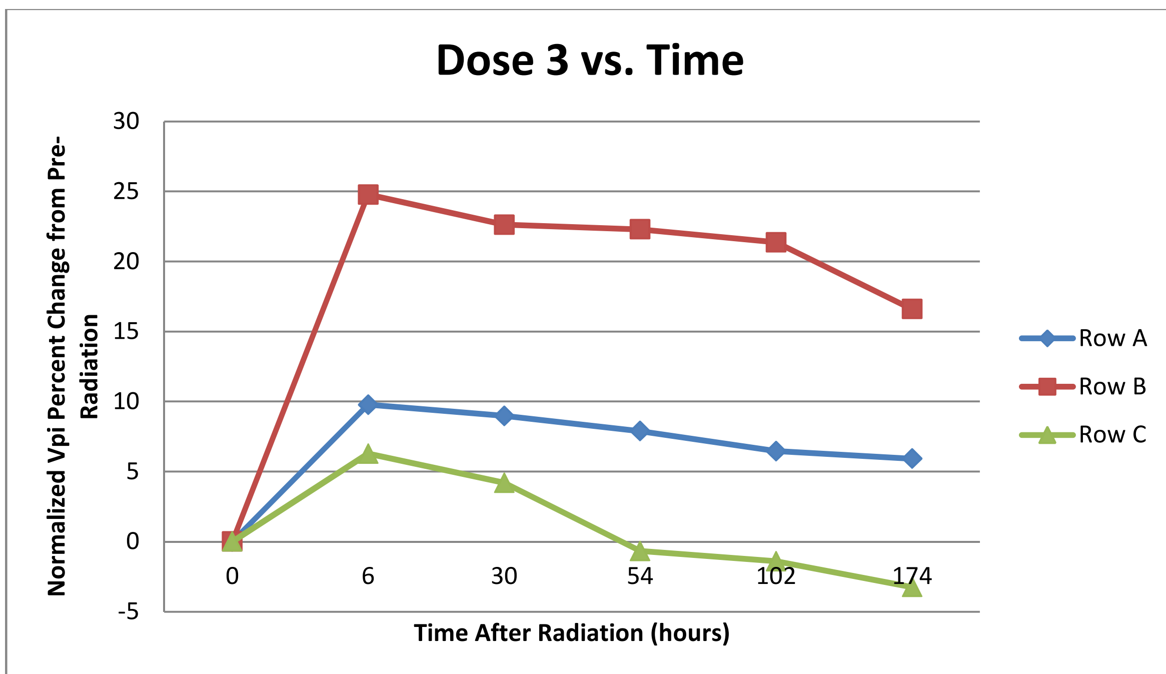

Fig.3b Dose 3 Radiation – Dose 3 devices showed a characteristic original spike in voltage followed by decay over time.

The decrease in V_{pi} occurring after the original spike is known to be caused by electron hole pair annihilation[6]. Positively charged holes tend to circulate through the dielectric layer until they come in contact with one of its interfaces. When a hole reaches an interface it will locate an electron and be annihilated. This leads to a positively charged dielectric layer degrading to a neutral charge over time. Physically speaking this decreases the V_{pi} necessary to displace the gate because of a decrease in repulsive electrostatic force.

Additional analysis was done to determine the effects of radiation on hysteresis - known as the voltage difference between pull in and release. Results however, showed no correlation between the two, instead a large and seemingly random distribution was obtained. This suggests that the pull out voltage might not be as dependent on electron hole pair accumulation. However, to verify this notion future research should be focused predominantly on the hysteresis.

Modeling the gate and dielectric as a parallel plate capacitor allows charge build up based on V_{pi} to be calculated:

$$\Delta Q = \frac{d}{\varepsilon A v_{pi-final}} - \frac{d}{\varepsilon A v_{pi-initial}}$$

Equation 7

Using this method the expected charge stored, calculated in equation 6, was two to six orders of magnitude greater than the actual charge stored for all devices (figures 4a & 4b). This reality is likely caused by the 900nm thick gate heavily shielding the relatively small, 80nm dielectric layer. Additionally it is unlikely that all or even most holes would be trapped. Rather the vast majority would likely find their counterpart instantly and annihilate.

	Device A	Device B	Device C
Dose 1	$2.6\ x\ 10^{-6}\ C$	$1.4\ x\ 10^{-6}\ C$	$6.5\ x\ 10^{-7}\ C$
Dose 2	$7.9\ x\ 10^{-5}\ C$	$4.2\ x\ 10^{-5}\ C$	$2.0\ x\ 10^{-5}\ C$
Dose 3	$2.6\ x\ 10^{-4}\ C$	$1.4\ x\ 10^{-4}\ C$	$6.5\ x\ 10^{-5}\ C$

Fig.4a Expected Charge Accumulation – Expected charge accumulation showed a high level of expected charge accumulation that would correspond to device shortage.

	Device A	Device B	Device C
Dose 1	$-5.1\ x\ 10^{-9}\ C$	$1.6\ x\ 10^{-8}\ C$	$1.6\ x\ 10^{-8}\ C$
Dose 2	$9.1\ x\ 10^{-10}\ C$	$9.3\ x\ 10^{-10}\ C$	$5.5\ x\ 10^{-10}\ C$
Dose 3	$4.3\ x\ 10^{-10}\ C$	$4.6\ x\ 10^{-10}\ C$	$2.3\ x\ 10^{-10}\ C$

Fig.4b Actual Charge Accumulation – Actual charge accumulated resulted in 10% - 30% V_{pi} *increases.*

IV. CONCLUSION

Despite radiation levels far in excess of natural space levels, the 6T relays tested showed acceptable fluctuations in V_{pi}. Interpolation of the data trends suggests that similar MEM devices should not have significant problems with radiation until the pull-in voltage has reached a level susceptible to the charge build-up. Even then the data indicates that only the most high dose radiation environments would be problematic.

It should, however, be noted that a probable cause for these levels of radiation hardness is likely the shielding effects of the gate. Similar devices without such a large layer covering the dielectric may well be much more susceptible to radiation. In fact, past research suggests that small MEM devices exposed to six magnitudes less of radiation have experienced more dramatic electrical effects. Thus, future fabricating and scaling of the 6T relays ought to maintain a focus on physical dimension ratios.

Radiation levels used in this experiment are many orders of magnitude higher than that which would be found in space over a comparable duration. Although this work suggests a great preventive mechanism for device degradation, it may be that annealing would play a significant role in practice. Low levels of radiation found aboard space

shuttles could theoretically be completely countered by materials with low annealing times. Even the most highly irradiated devices in this experiment showed substantial annealing potential over the span of a week. In practice these devices would receive the same levels of irradiation over many years, suggesting that they would anneal at a rate quick enough to reverse any hole pair generation in short order.

Ultimately, current 6T relay technology is highly robust, as demonstrated by favorable reactions under extremely high doses of radiation. This technology would be a viable option for future spacecraft projected for travel to any known part of the universe.

V. REFERENCES

[1] M. Spencer, F. Chen, C. Wang, R. Nathanael, H. Fariborzi, A. Gupta, H. Kam, V. Pott, J. Jeon, T. King-Liu, D. Markovic, E. Alon and V. Stojanovic, "Demonstration of Integrated Micro-Electro-Mechanical Relay Circuits for VLSI Apllications," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp 308-320, Jan. 2011.

[2] H. Shea, "Reliability of MEMS for space applications," *Ecole Polytechnique Federale de Lausanne*, rue Jaquet Droz 1, 2011.

[3] J. Caffey, P. Kladitis, "The effects of ionizing radiation on microelectromechanical systems (MEMS) actuators: electrostatic, electrothermal, and bimorph," *IEEE Micro Electro Mechanical Systems*, 17th international conference on MEMS, pp 133-136, Sep. 2004.

[4] S. McClure, L. Edmonds, R. Mihailovich, A. Johnston, P. Alonzo, J. DeNatale, J. Lehman, C. Yui, "Radiation effects in micro-electromechanical systems (MEMS): RF relays," *Nuclear Science*, vol. 49, no. 6, pp 3197-3202, Jan. 2003.

[5] H. Shea et al., "Effects of Electrical Leakage Currents on MEMS Reliability and Performance," IEEE Transactions on Devicee and Materials Reliability, vol. 4, no. 2, pp 198, 2004.

[6] R. Powell, "Vacuum-ultraviolet-induced space charge in Al_2O_3 films," applied *physics letters*, vol. 28, no. 11, Jun. 1976.

VI. ACKNOWLEDGEMENTS

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Quality Assurance of Electrostatic Micro-Electro Mechanical Relays: Radiation Hardness

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Requisite Thesis Signatures

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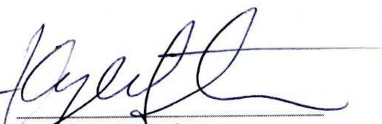

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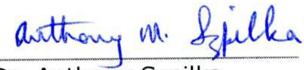

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